C²I² Systems

CCII Systems (Pty) Ltd Registration No. 1990/005058/07

Communications
Computer Intelligence
Integration

User Manual
for
C²I² Systems
2-Channel Serial I/O PMC Adapter
and
GPS PMC Adapter

C²I² Document No.	CCII/LCP/6-MAN/001
Document Issue	1.1
Issue Date	2003-09-11
Print Date	2003-09-11
File Name	W:\LCP\TECH\MAN\CLCMAN01.WPD
Distribution List No. :	

Signature Sheet

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Amendment History

Issue	Description	Date	ECP No
0.1	First Draft	2002-06-28	-
0.2	Revised according to review	2002-07-17	-
0.3	Updated to reflect schematic changes for EXAR IC	2002-09-18	CCII/LCP/6-ECP/001
0.4	Added NMEA sentences and updated as per WRM review	2002-12-02	-
1.0	Reviewed NMEA sentences	2002-12-18	-
1.1	Updated to include conduction-cooled board	2003-09-11	CCII/LCP/6-ECP/007

Contents

Abbreviations and Acronyms

ASCII	American Standard Code for Information Interchange
dB	deciBel
BIST	Built In Self Test Register
CCII	CCII Systems (Pty) LTD
CD	Carrier Detect
CS	Chip Select
CTS	Clear to Send
DTE	Data Terminal Equipment
DGPS	Differential GPS
DSR	Data Set Ready
DTR	Data Terminal Ready
E	East
FIFO	First In First Out memory structure
GPS	Global Positioning System
Hz	Hertz
I/O	Input / Output
INT	Interrupt
IRQ	Interrupt Request
LSB	Least Significant Bit
MSB	Most Significant Bit
N	North
NMEA	National Marine Electronics Association
PCI	Peripheral Component Interconnect
PMC	PCI Mezzanine Card
RI	Ring Indicator
RTCM	Radio Technical Commission for Maritime Services
RTS	Request To Send
RX	Receive
S	South
SNR	Signal to Noise Ratio
SV	Satellites in View
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
UTC	Coordinated Universal Time
W	West

1. Scope

This document serves as a user manual for the C²I² Systems 2-Channel Serial I/O PMC Adapter and GPS PMC Adapter.

1.1 Introduction

The 2-Channel Serial I/O PMC Adapter provides two full duplex, asynchronous serial ports. Both ports are capable of transmitting and receiving data using RS-232 standards. Only one of the serial ports is available on the GPS PMC Adapter. The other serial port is used to interface to another GPS module for the purposes of implementing Differential GPS (DGPS).

These PMC Adapters adhere to the electrical requirements of the PCI interface specification and to the mechanical requirements of the PMC interface standard.

2. References

2.1 Specifications

2.1.1 CMC P1386, *Draft Standard for a Common Mezzanine Card Family*, Draft 2.0, 1995-04-04
2.1.2 NMEA 0183, *Standard for Interfacing Marine Electronic Equipment*, Version 3.01, 2002-01-01
2.1.3 NMEA 0183 HS, *High Speed Addendum to NMEA 0183 Interface Standard*, Version 3.01, 2002-01-01
2.1.4 *PCI Local Bus Specification*, Revision 2.1, 1995-06-01
2.1.5 PMC, P1386.1, *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards*, Revision 2.0, 1995-04-04
2.1.6 RTCM Special Committee No. 104, *RTCM Recommended Standards for Differential NAVSTAR GPS Service*, Version 2.1, 1994-01-01

3. System Overview

The block diagrams of the PMC Adapters are shown below :

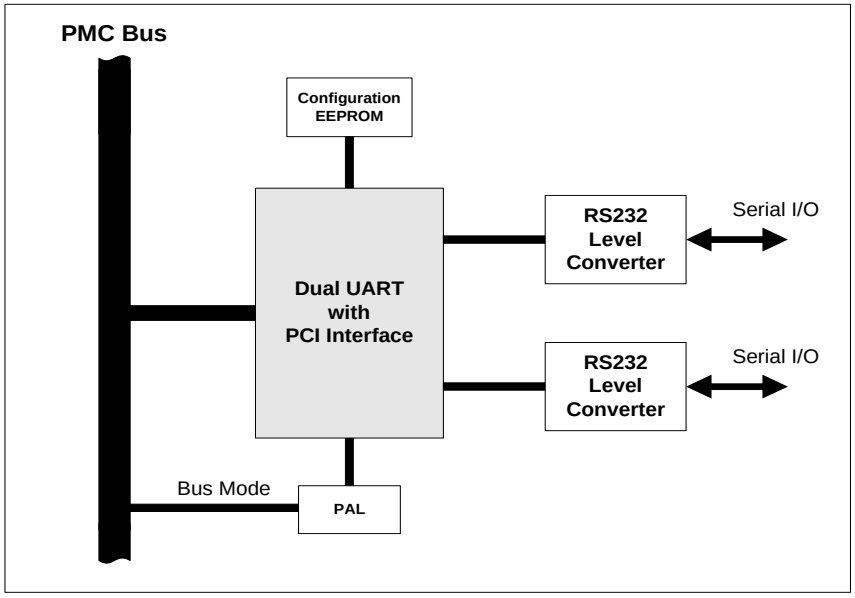


Figure 1 : 2-Channel Serial I/O PMC Adapter

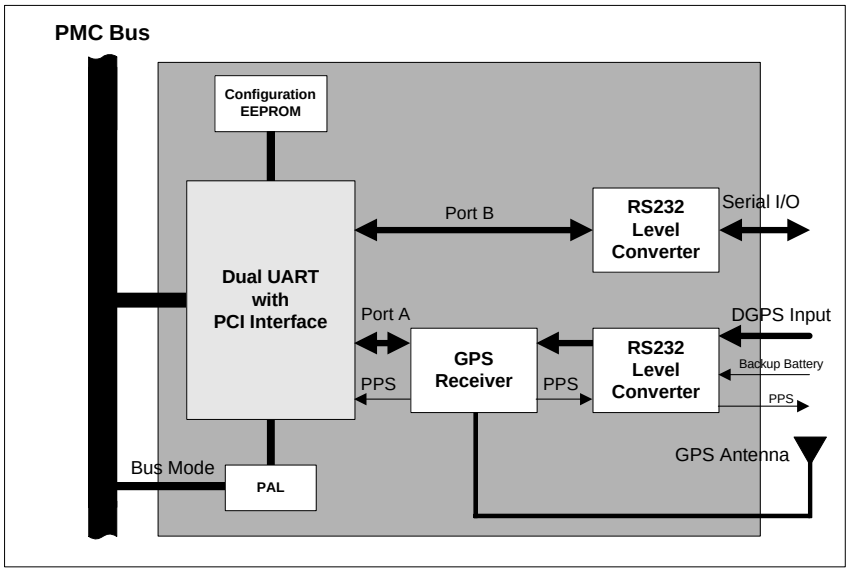


Figure 2 : GPS PMC Adapter

The two systems are essentially the same. However, when the GPS receiver is installed (as on the GPS PMC Adapter), the second RS-232 port is dedicated to GPS functionality.

4. PMC/PCI Interface

4.1 Overview

Both the 2-Channel Serial I/O PMC Adapter and the GPS PMC Adapter conform to the PMC interface specification which is based on the PCI bus interface standard.

The PMC interface standard defines the physical and environmental aspects of the PCI mezzanine card interface. The PMC Adapters implement a single width module that can provide I/O through either a DB25 front panel connector or through the back plane connector.

The PCI interface standard defines the electrical aspects of the interface. The PMC Adapters provide a PCI compliant slave interface allowing the host board to transfer data to and from the serial interface controller.

The PCI interface is implemented using a PCI based dual-channel UART bridge.

4.2 Configuration Space

The PCI interface defines a standard programming model for the configuration of PCI devices. This interface is defined as the *Configuration Space*.

The table below shows the Configuration Space as defined by the PCI bus specification :

AD31-23	AD22-16	AD15-8	AD7-0	Address
Device ID(0x0152)		Vendor ID(0x13A8)		0x00
Status		Command		0x04
Class Code(0x070002)			Revision ID(0x01)	0x08
BIST	Header Type	Latency Timer	Cache Size(08)	0x0C
Memory Base Address Register (BAR)				0x10
Unimplemented Base Address Register				0x14
Unimplemented Base Address Register				0x18
Unimplemented Base Address Register				0x1C
Unimplemented Base Address Register				0x20
Unimplemented Base Address Register				0x24
Reserved				0x28
Subsystem ID		Subsystem Vendor ID		0x2C
Reserved				0x30
Reserved				0x34
Reserved				0x38
Max Latency(0x00)	Min Grant(0x00)	Interrupt Pin(0x01)	Interrupt Line	0x3C

The location of the configuration registers is defined by the host board. The host board assigns a specific address line to the module interface by connecting it to the IDSEL pin on the PMC interface. To determine the configuration registers locations refer to the manual of the host board.

4.3 PCI Interrupts

The PMC Adapters supports interrupts on the INTA# pin only. This is reflected in the *Interrupt Pin Register* of the Configuration Space as defined in section 4.2.

4.4 PMC Connectors

The PMC Adapters are fitted with two connectors (P11 and P12) to implement the 32-bit PMC interface. The board may be fitted with a either connector P14 (required for back plane connection to the interface signals) or the front panel connector (JP2). J1 is the connector for the GPS antenna on the GPS PMC Adapter. The front and rear panel configurations are shown below :

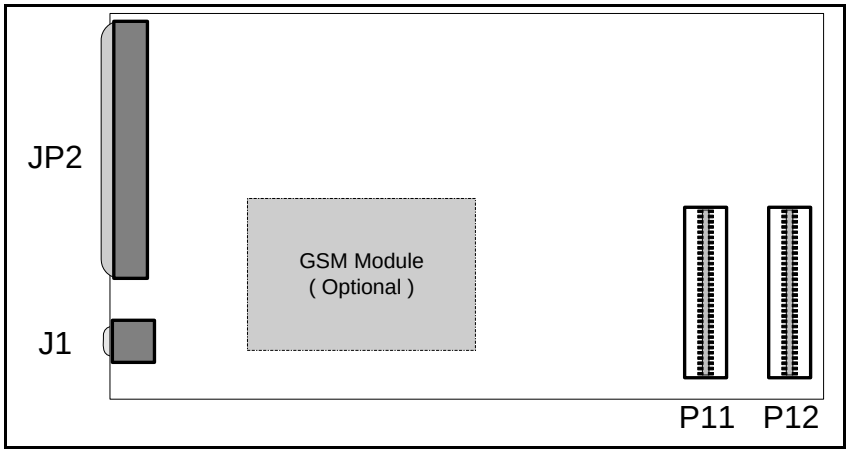


Figure 3 : Front Panel I/O Configuration

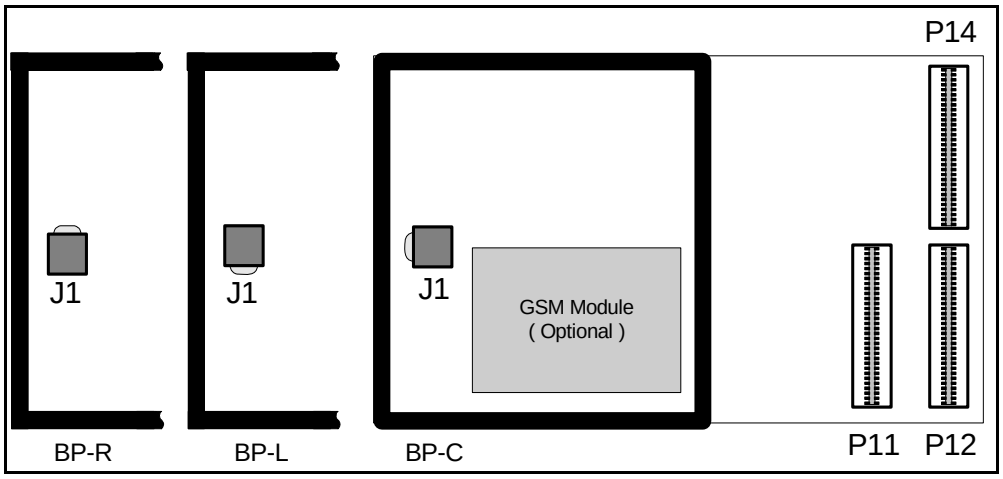


Figure 4 : Rear Panel I/O Configuration

4.5 PMC Pin Assignments

The PMC Adapters have the following PMC connections (note that P14 is only for the rear panel configuration) :

P11 Signals			
Pin	Signal Name	Signal Name	Pin
1	TCK	-12V	2
3	Ground	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	PCI-RSVD	10
11	Ground	PCI-RSVD	12
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5V	18
19	V (I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V (I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5V	38
39	Ground	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	Ground	44
45	V (I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	V (I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64#	64

P12 Signals			
Pin	Signal Name	Signal Name	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD	8
9	PCI-RSVD	PCI-RSVD	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE3#	14
15	+3.3V	BUSMODE4#	16
17	PCI-RSVD	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PMC-RSVD	34
35	TRDY#	+3.3V	36
37	Ground	STOP#	38
39	PERR#	Ground	40
41	+3.3V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PMC-RSVD	52
53	+3.3V	PMC-RSVD	54
55	PMC-RSVD	Ground	56
57	PMC-RSVD	PMC-RSVD	58
59	Ground	PMC-RSVD	60
61	ACK64#	+3.3V	62
63	Ground	PMC-RSVD	64

P14 Signals (Rear Panel Configuration Only)					
Pin	Direction	Signal Name	Signal Name	Direction	Pin
1	Output	TX_A / TX_DGPS	DTR_A	Output	2
3	Output	RTS_A	CD_A	Input	4
5	Input	RX_A / RX_DGPS	DSR_A	Input	6
7	Input	CTS_A	RI_A	Input	8
9	Output	TX_B	DTR_B	Output	10
11	Output	RTS_B	CD_B	Input	12
13	Input	RX_B	DSR_B	Input	14
15	Input	CTS_B	RI_B	Input	16
17	Output	GPS Pulse Per Second	GPS Battery Backup	Input	18
:		**NOT USED**			:
59		Ground	Ground		60
61		Ground	Ground		62
63		Ground	Ground		64

Note : P14 Signals are all RS-232 level compliant signals. Furthermore, the signals are configured such that the Adapters are DTE's. This implies that TX lines are outputs and RX lines are inputs with respect to the PMC Adapters.

5. Serial Interface

5.1 Overview

The PMC Adapters have either one (GPS PMC Adapter) or two (2-Channel Serial I/O PMC Adapter) asynchronous RS-232 serial ports. Programming registers for these ports are compatible with the 16C550 UART. The ports are configured as below :

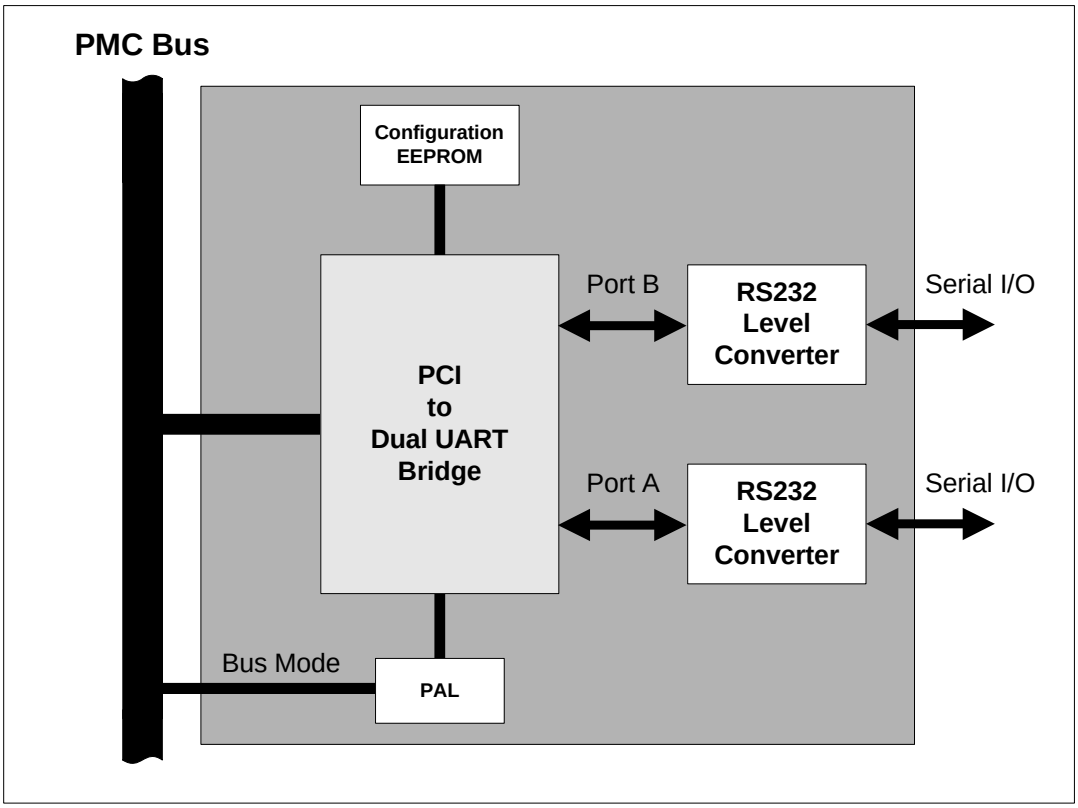


Figure 5 : Serial Interface

One the Rear panel PMC Adapter, the signals are available at P14 as detailed in section 4.4.

On the front panel PMC Adapters, the signals are available at JP2 (a DB25 connector as shown in section 4.4). The pinout is as show in the table below :

J2 Signals (DB25 Connector - Front Panel Configuration Only)		
Pin	Direction	Signal Name
1		GND
2	Output	DTR_B
3	Output	TX_B
4	Input	RX_B
5	Input	CD_B
6		GND
7	Output	GPS Pulse Per Second
8	Input	GPS Battery Backup
9		GND
10	Output	DTR_A
11	Output	TX_A/RX_DGPS
12	Input	RX_A/TX_DGPS
13	Input	CD_A
14	Input	RI_B
15	Input	CTS_B
16	Output	RTS_B
17	Input	DSR_B
18		NOT USED
19		NOT USED
20		NOT USED
21		NOT USED
22	Input	RI_A
23	Input	CTS_A
24	Output	RTS_A
25	Input	DSR_A

Note : J2 Signals are all RS-232 level compliant signals. Furthermore, the signals are configured such that the Adapters are DTE's. This implies that TX lines are outputs and RX lines are inputs with respect to the PMC Adapters.

5.2 Memory Map

The memory map for the UART registers are given in the table below :

Offset Address	Memory Space	Read/Write	Comment
0x000-0x00F	UART channel A registers		16C550 compatible
0x100	UART A - Read FIFO	Read-Only	64 bytes of RX FIFO
0x100	UART A - Write FIFO	Write-Only	64 bytes of TX FIFO
0x200-0x20F	UART channel B registers		16C550 compatible
0x300	UART B - Read FIFO	Read-Only	64 bytes of RX FIFO
0x300	UART B - Write FIFO	Write-Only	64 bytes of TX FIFO

5.3 UART Register Descriptions

5.3.1 Transmitter Holding Register (THR)

The transmitter section consists of a transmitter holding register (THR) and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO.Transmitter section control is a function of the UART line control register. The UART THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at TX. In the 16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER-1=1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

5.3.2 Receive Holding Register (RHR)

The receiver section of the UART consists of a receiver shift register (RSR) and a receiver Holding register (RHR). The RHR is actually a 16-byte FIFO. Timing to receive holding register is supplied by the 16xreceiver clock. Receiver section control is a function of the UART line control register. The UART RHR receives serial data from RX. The RSR then concatenates the data and moves it into the RHR FIFO. In the 16C450 mode, when a character is placed in the receiver holding register and the received data available interrupt is enabled (IER-0=1), an interrupt is generated. This interrupt is cleared when the data is read out of the receiver holding register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

5.3.3 Interrupt Enable Register (IER)

The interrupt enables register enables each of the five types of interrupts and INT pin response to an interrupt generation. The interrupt enable register can also be used to disable the interrupt system by setting bits 0-3 to logic 0. The contents of this register are described below.

IER Bit-0 :

0 = Disable the received data available interrupt.

1 = Enables the received data available interrupt.

IER Bit-1 :

0 = Disable the transmitter holding register empty interrupt.

1 = Enable the transmitter holding register empty interrupt.

IER Bit-2 :

0 = Disables the receiver line status interrupt.

1 = Enables the receiver line status interrupt.

IER Bit-3 :

0 = Disables the modem status interrupt.

1 = Enables the modem status interrupt.

IER Bit 4 :

0 = Standard 16C450/550 mode. Sleep mode is disabled.

1 = Enables Sleep mode. The UART is always awake when there is a byte in the transmitter, activity on the RX, or either Delta CTS, Delta DSR, Delta CD, Delta RI is/are set to logic "1", or when the device is in the loopback mode.

IER Bit 5 :

0 = Standard 16C450/550 mode. Power down mode is disabled.

1 = Enables the power down mode. Power down mode functions similar to Sleep mode, except oscillator section.

IER Bits 6-7 :

These bits are not used (always set to 0).

5.3.4 Interrupt Identification Register (IIR)

The UART has an on chip interrupt generation and prioritization capability.

IIR Bit-0 :

0 = An interrupt is pending. Used either in a hardware prioritized or polled interrupt system.

1 = No interrupt is pending.

IIR Bits 1-2 :

The UART provides four prioritized levels of interrupts :

- Priority 1 - Receiver line status (highest priority)
- Priority 2 - Receiver data ready
- Priority 2 - Receiver character time-out
- Priority 3 - Transmitter holding register empty
- Priority 4 - Modem status (lowest priority)

When an interrupt is generated, the interrupt identification register indicates that an interrupt is pending and encodes the type of interrupt in its three least significant bits (bits 0, 1, and 2).

Interrupt Priority decode

Bit-3	Bit-2	Bit-1	Bit-0	Interrupt source
0	1	1	0	Receive Data Error
0	1	0	0	Receive Data Ready
1	1	0	0	Receive Time-Out
0	0	1	0	Transmit Holding Empty
0	0	0	0	Modem Status Change

These bits are used to identify the highest priority interrupt pending.

IIR Bit-0 will clear to "1" when no interrupt is pending. To clear the interrupts it is necessary to perform reads from the following registers as required.

- **Receive Data Error :** Reading LSR register will clear this interrupt. User should save LSR value after reading the register to maintain the error condition.
- **Receive Data Ready :** Reading RHR register till FIFO becomes empty.
- **Receive Timeout :** Reading entire characters from RHR.
- **Transmit Holding Empty :** Writing a character into THR register or reading IIR register (if source of interrupt).
- **Modem Status Change :** Reading MSR register will clear this interrupt.

IIR Bit-3 :

0 = In the 16C450 mode. In FIFO mode, this bit is set along with bit-2 to indicate that a time-out interrupt is pending.

IIR Bit 4 :

This bit is not used (always reset at 0).

IIR Bit 5 :

0 = 16C450/550 mode, 16 byte FIFO mode.

1 = Enhance FIFO mode. 64 byte FIFO mode enabled.

IIR Bits 6-7 :

0 = In the 16C450 mode.

1 = When FCR-0 is equal to 1.

5.3.5 FIFO Control Register (FCR)

The FIFO control register (FCR) is a write only register. The (FCR) enables and clears the FIFO sets receive FIFO trigger level, and selects the type of DMA signaling.

FCR Bit-0 :

0 = 16C450 mode, disables the transmitter and receiver FIFO.

1 = Enables the transmitter and receiver FIFO. This bit must be set to 1 when other (FCR) bits are written to or they are not programmed. Changing this bit clears the FIFO.

FCR Bit-1 :

0 = Normal operation

1 = Clears all bytes in the receiver FIFO and resets its counter logic to 0. The shift register is not cleared. The one that is written to this bit position is self-clearing.

FCR Bit-2 :

0 = Normal operation

1 = Clears all bytes in the transmit FIFO and resets its counter logic to 0. The shift register is not cleared. The one that is written to this bit position is self-clearing.

FCR Bit-3 :

0 = Mode [0] : Supports single transfer DMA (16C450 mode) in which a transfer is made between Host bus cycle.

1 = Mode [1] : Supports multi transfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied.

FCR Bit 5-4 :

These bits are not used.

FCR Bits 6-7 :

These bits are used to set the trigger level for receive FIFO interrupt.

Receive Trigger Levels (Bytes)

Bit-7	Bit-6	RX FIFO Trigger Level
0	0	1
0	1	4
1	0	8
1	1	14

5.3.6 Line Control Register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the line control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the line control register; this eliminates the need for separate storage of the line characteristics in system memory.

LCR Bits 0-1 :

These two bits specify the number of bits in each transmitted or received serial character.

Word Length

Bit-1	Bit-0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

LCR Bit-2 :

This bit specifies, 1, 1-1/2, or 2 stop bits in each transmitted character. When bit-2 is reset to 0, one stop bit is generated in the data. When bit-2 is set to 1, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit-2.

Stop Bits

Bit-2	Word Length	Stop Bit(s)
0	X	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

LCR Bit-3 :

0 = Parity is disabled. No parity is generated or checked.

1 = Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, parity is checked.

LCR Bit-4 :

0 = ODD parity select bit. When parity is enabled by bit-3, a 1 in bit-4 produces odd parity (an odd number of 1's in the data and parity bits.

1 = Even parity select bit. When parity is enabled by bit-3, a 1 in bit-4 produces even parity (an even number of 1's in the data and parity bits).

LCR Bit-5 :

0 = Stick parity is disabled.

1 = Stick parity bit. When bits 3-5 are set to 1 the parity bit is transmitted and checked as a 0. When bits-3 and 5 are 1's and bit-4 is a 0, the parity bit is transmitted and checked as 1.

Parity Selection

Bit-5	Bit-4	Bit-3	Parity Type
X	X	0	No Parity
0	0	1	Odd Parity
0	1	1	Even Parity
1	0	1	Forced Parity “1"
1	1	1	Forced Parity “0"

LCR Bit-6 :

0 = Normal operation. Break condition is disabled and has no effect on the transmitter logic.

1 = Force a break condition. A condition where TX is forced to the space (low) state.

LCR Bit-7 :

0 = Normal operation.

1 = Divisor latch enable. Must be set to 1 to access the divisor latches of the baud generator during a read or write. Bit-7 must be reset to 0 during a read or write to the receiver holding, the transmitter holding register, or the interrupt enable register.

5.3.7 Modem Control Register (MCR)

The modem control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem.

MCR Bit-0 :

0 = Sets the DTR output pin to the mark (high) state.

1 = Sets the DTR output pin to the space (low) state.

MCR Bit-1 :

0 = Sets the RTS output pin to the mark (high) state.

1 = Sets the RTS output pin to the space (low) state.

MCR Bit-2 :

0 = Sets the OP1 to the mark (high) state during loop-back mode.

1 = Sets the OP1 to the space (low) state during loop-back mode.

MCR Bit-3 :

0 = Disables UART interrupt. Sets the OP2 to mark (high) during loop-back mode.

1 = Enables UART interrupt. This bit is gated with IER Bits 0-3. Sets the OP2 to the space (low) state during loop-back mode.

MCR Bit-4 :

0 = Normal operation.

1 = Internal loop back mode. Provides a local loop-back feature for diagnostic testing of the UART. When LOOP is set to 1, the following occurs :

- The transmitter TX pin is set to the mark (high) state.
- The receiver RX pin is disconnected.
- The output of the transmitter shift register is looped back into the receiver shift register input.
- The four modem inputs (CTS, DSR CD and RI) pins are disconnected.
- The four modem outputs (DTR, RTS, OP1, OP2) pins are internally connected to the four modem inputs.
- The four modem outputs are forced to the mark (high) state.

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify transmit and receive data paths to the UART. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt sources are now the lower four bits of the modem control register instead of the four modem control inputs. All interrupts are still controlled by the interrupt enable register.

MCR Bit-5 :

0 = 16C450/550 mode. Hardware flow control is disabled.

1 = Enable hardware flow control (RTS/CTS).

Flow Control

Bit-5	Bit-1	Flow Control
1	1	Auto RTS/CTS
1	0	Auto CTS only
0	X	Disabled

RTS becomes active (space state) when the receiver is empty or the threshold has not been reached. When receiver FIFO level reaches a trigger level of 1, 4, 8, and 14, RTS is de-asserted (mark state). RTS is automatically reasserted once the receiver FIFO is empty by reading receive holding register. The transmitter circuitry checks CTS before sending the next data byte. When CTS is active (space state), the transmitter sends the next byte. To stop the transmitter from sending the next byte, CTS must be released before the middle of the last stop bit that is currently being sent.

MCR bits 6-7 :

These bits are not used.

5.3.8 Line Status Register (LSR)

The line status register provides information to the Host concerning the status of data transfers. The line status register is intended for read operations only; writing to this register is not recommended. Bits 1-4 are the error conditions that produce a receiver line status interrupt.

LSR Bit-0 :

0 = No data in receive holding or FIFO.

1 = Data ready indicator for the receiver. This bit is set to 1 whenever a complete incoming character has been received and transferred into the receiver holding register or the FIFO. It is reset to 0 by reading all of the data in the receiver holding register or the FIFO.

LSR Bit-1 :

0 = Normal operation. No overrun error.

1 = It indicates that before the character in the receiver holding register was read, it was over written by the next character transferred into the register. OE is reset every time the Host reads the contents of the line status register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the Host as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR Bit-2 :

0 = Normal operation (No parity error).

1 = It indicates that the parity of the received data character does not match the parity selected in the line control register. PE is reset every time the Host reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the Host when its associated character is at the top of the FIFO.

LSR Bit-3 :

0 = Normal operation (No framing error).

1 = It indicates that the received character did not have a valid stop bit. FE is reset every time the Host reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the Host when its associated character is at the top of the FIFO. The UART tries to re-synchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit.

LSR Bit-4 :

0 = Normal operation.

1 = It indicates that the received data input was held in the logic space (low) state for longer than a full word transmission time. A full word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is reset every time the Host reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the Host when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO.

LSR Bit-5 :

0 = At least one byte is written to the transmit FIFO or transmit holding register.

1 = Transmitter holding register is empty, indicating that the UART is ready to accept a new character. If the THRE interrupt is enabled when THRE is set to 1, an interrupt is generated. THRE is set to 1 when the contents of the transmitter holding register are transferred to the transmitter shift register.

LSR Bit-6 :

0 = When either the transmitter holding register or the transmitter shift register contains a data character.

1 = Transmitter holding register and the transmitter shift register are both empty.

LSR Bit-7 :

0 = In the 16C450, this bit is always reset to 0.

1 = In the FIFO mode, at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

5.3.9 Modem Status Register (MSR)

The modem status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the Host. Additionally, four bits of this register provide change information, when input from the modem Changes State, the appropriate bit is set to 1. All four bits are reset to 0 when the Host reads the modem status register.

MSR Bit-0 :

0 = No change to CTS input.

1 = Indicates that the CTS input has changed state since the last time it was read by the Host. When interrupt is enabled, a modem status interrupt is generated.

MSR Bit-1 :

0 = No change to DSR input.

1 = Indicates that the DSR input has changed state since the last time it was read by the Host. When interrupt is enabled, a modem status interrupt is generated.

MSR Bit-2 :

0 = No change to RI input.

1 = Indicates that the RI input has changed from the space (low) state to the mark (high) state. When RI is set to the mark (high) state and the modem status interrupt is enabled, a modem status interrupt is generated.

MSR Bit-3 :

0 = No change to CD input.

1 = Indicates that the CD input has changed state since the last time it was read by the Host. When interrupt is enabled, a modem status interrupt is generated.

MSR Bit-4 :

Complement of the clear to send (CTS) input. When the UART is in the diagnostic test mode, this bit is equal to RTS.

MSR Bit-5 :

Complement of the data set ready (DSR) input. When the UART is in the diagnostic test mode, this bit is equal to DTR.

MSR Bit-6 :

Complement of the ring indicator (RI) input. When the UART is in the diagnostic test mode, this bit is equal to OP1.

MSR Bit-7 :

Complement of the data carrier detects (CD) input. When the UART is in the diagnostic test mode, this bit is equal to OP2.

5.3.10 Scratch Pad Register (SPR)

The scratch pad register is an 8-bit register that is intended for programmer use as a scratch pad in the sense that it temporarily holds the programmer data without affecting any other UART operation.

5.3.11 Programmable Buad-Rate Generator

Each UART has its own Baud-Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescalar is controlled by a software bit in the MCR register. The MCR register bit 7 sets the prescalar to divide the on-board clock (14.7456 MHz) by 1 or 4. The output of the prescalar clocks the BRG. The BRG further divides the clock to a programmable divisor between 1 and (2^{16}-1) to obtain a 16X or 8X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up. Therefore, the BRG must be programmed during initialization to the operating data rate.

Baud Rate Generator Programming

Baud Rate MCR Bit7=1	Baud Rate MCR Bit7=0	Divisor for 16X Clock (Hex)	DLM (Hex)	DLL (Hex)
600	2400	180	1	80
1200	4800	0C0	0	C0
2400	9600	060	0	60
4800	19.2k	030	0	30
9600	38.4k	018	0	18
19.2k	76.8k	00C	0	0C
38.4k	153.6k	006	0	06
57.6k	230.4k	004	0	04
115.2k	460.8k	002	0	02

5.3.12 FIFO Interrupt Mode Operation

When the receiver FIFO and receiver interrupts are enabled (FCR-0=1, IER-0=1, IER-2=1), a receiver interrupt occurs as follows :

The received data available interrupt issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.

The receiver line status interrupt has higher priority than the received data available interrupt. The data ready bit (LSR-0) is set when a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled, FIFO time-out interrupt occurs when the following conditions exist :

At least one character is in the FIFO. The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay). The most recent microprocessor read of the FIFO occurred more than five continuous character times ago. When a time-out interrupt has occurred, it is cleared and the timer is reset when the microprocessor reads one character from the receiver FIFO. When a time-out interrupt has not occurred, the timeout timer is reset after a new character is received or after the microprocessor reads the receiver FIFO. When the transmitter FIFO and THRE interrupt are enabled (FCR-0=1, IER-1=1), transmit interrupts occur as follows :

The occurrence of transmitter holding register empty interrupt is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time the transmitter FIFO was empty. It is cleared as soon as the transmitter holding register is written to (1 to 64 characters may be written to transmit FIFO while servicing this interrupt) or the IIR is read. The first transmitter interrupt after changing FCR is immediate if it is enabled.

The transmitter empty indicator is delayed one character time when there has not been at least two bytes in the transmitter FIFO at the same time since the last time that TEMT=1. TEMT is set after the stop bit has been completely shifted out.

The transmitter FIFO empty indicator works the normal way in this mode and is not delayed. Character timeout and receiver FIFO trigger-level interrupts have the same priority as the current received data available interrupt.

5.3.13 Register Reset Conditions

The value of the registers at reset is given below.

Reset Conditions

Register	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
RHR	X	X	X	X	X	X	X	X
THR	X	X	X	X	X	X	X	X
IER	0	0	0	0	0	0	0	0
FCR	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	1	1	0	0	0	0	0	0
MSR	X	X	X	X	0	0	0	0
SPR	1	1	1	1	1	1	1	1

6. **GPS Interface**

6.1 Overview of GPS Interface

On the GPS PMC Adapter, Port A is dedicated to GPS functionality. Hence, Port A is no longer available for user communication purposes.

The ports are configured as below :

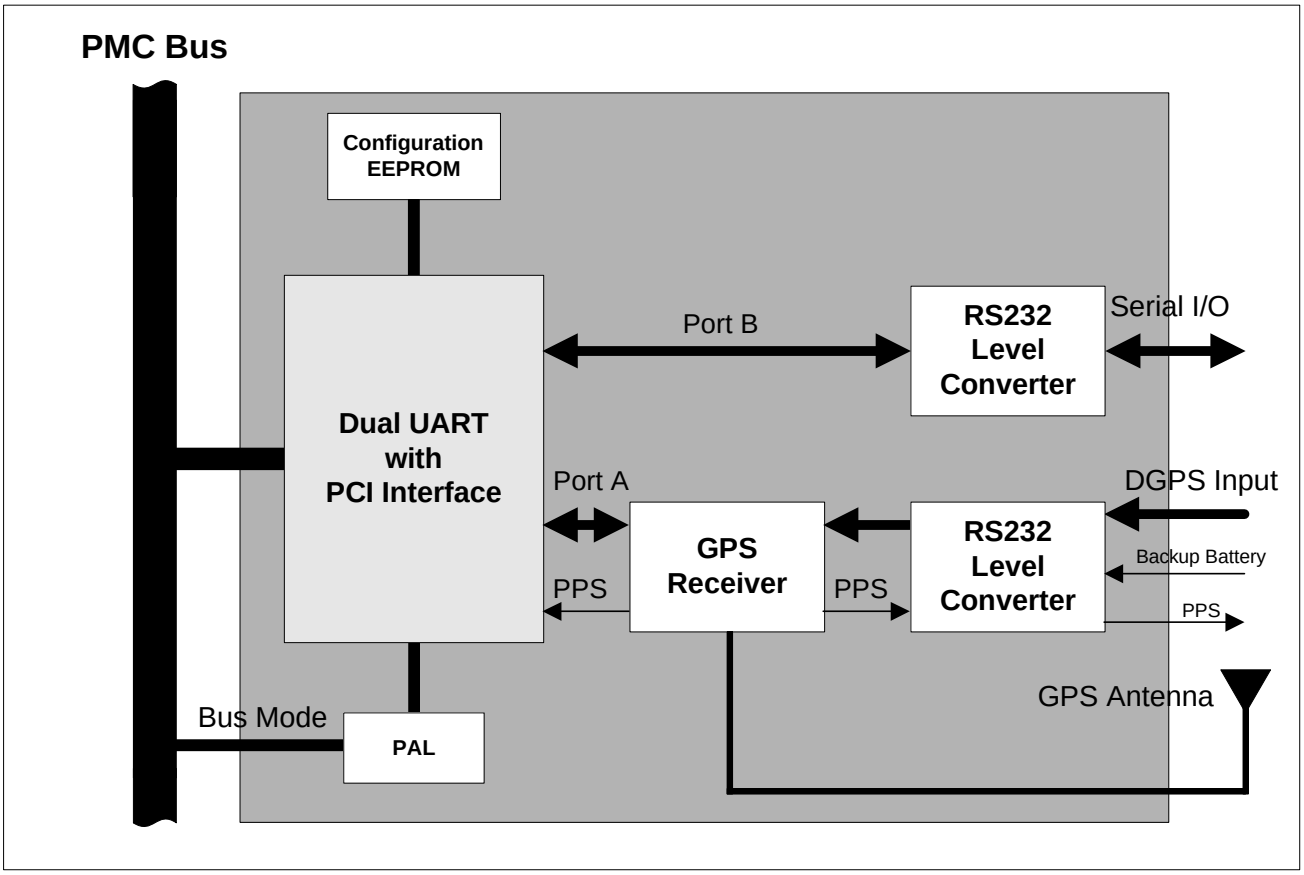


Figure 6 : GPS PMC Adapter

DGPS I/O signals can be found on connector JP2 (a DB25 connector as shown in section 4.4). The pinout is as shown in section 5.1. The GPS antenna is connected to connector J1 (as shown in section 4.4).

6.2 GPS Receiver Specifications

The GPS receiver module incorporated into the design is the µ-blox TIMA-B001. The table below summarises the specifications of the GPS receiver module :

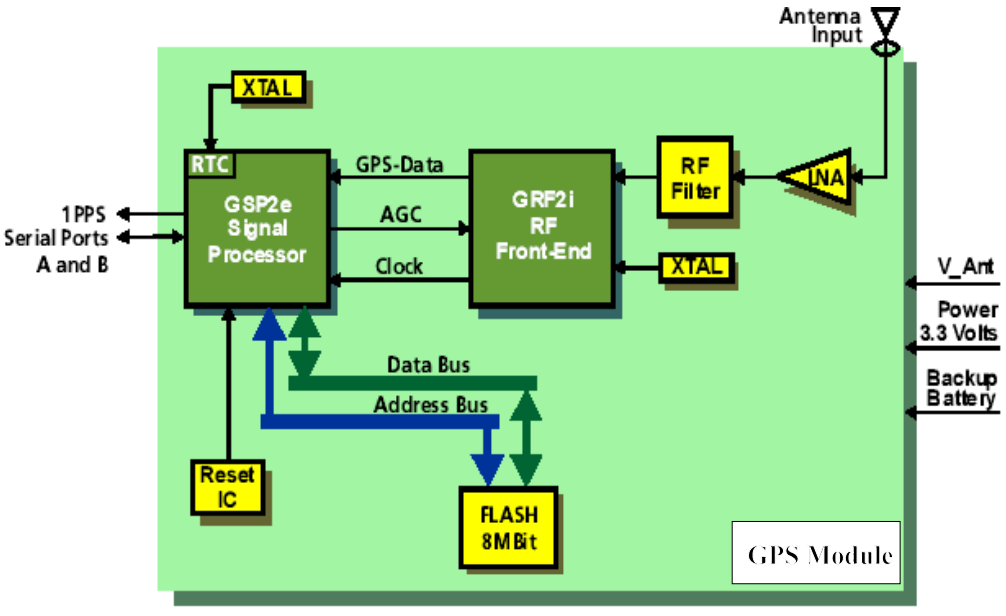
GPS Receiver Module Specifications

Parameter	Specification	
Receiver Type	L1 frequency, C/A Code, 12 Channel	
GPS Data Format	NMEA	
DGPS Correction Data Format	RTCM	
Max Update Rate	1 Hz	
Accuracy (SA off)	Position 4 m CEP	
Accuracy (DGPS, Accuracy off)	Position < 2 m CEP	
Acquisition (Typical)	Cold Start	45 s (typical)
	Warm Start	38 s (typical)
	Hot Start	< 8 s (typical)
Signal Reacquisition	<100 ms	
Receive/Transmit Baud Rates	4800,9600,19200,38400*	
Dynamics	<= 4g	
Operating Limits	Altitude < 18000 m, Velocity < 515 m/s (Either limit may be exceeded but not both - COCOM restrictions)	
Backup Battery	1.85 V to 3.6 V with a typical current consumption of 4.5 µA	

* NMEA allows using baud rates down to 4800 depending on the messages used.

6.3 Architecture of GPS Receiver Module

The diagram below shows the block diagram of the GPS receiver module incorporated in the system :



6.4 Default Configuration

The GPS receiver module has the following default configuration :

- Data read is in the NMEA format. The following sentences are generated by default : GLL, GGA, RMC, VTG, GSV, GSA.
- Position fixes are generated at the maximum update rate.
- Differential Configuration Data received from the DGPS port is according to the RTCM SC-104 standard.
- Transfer protocol is 9600 baud, 8 data bits, no parity, 1 stop bit.

6.5 Configuration

The GPS receiver module is connected to Port A. Hence, Port A should be configured with the same parameters (ie. baud rate, number of stop bits, parity etc) as the GPS receiver module.

The GPS receiver module communicates using the NMEA protocol (consult the NMEA 0183 Interface Standard). DGPS Correction Data is received using the RTCM protocol (consult the RTCM SC-104 Standard).

6.6 External Backup Battery

Use of an external backup battery is recommended to reduce the acquisition time of the GPS module. If an external backup battery is connected, the module keeps the internal Real Time Clock running and holds the SRAM data (ephemeris and almanac) during power supply interruption. This enables warm and hot start. However, under good visibility conditions cold and warm start times do not differ significantly.

Connection of an external backup battery is made via the rear panel connector (P14 pin 18) or the front panel connector (JP2 pin 8). The external backup battery must be capable of delivering 1.85 V to 3.6 V with a typical current consumption of 4.5 µA.

Should an external backup battery not be connected, the user must ensure that this signal is grounded either on P14 or JP2.

6.7 Pulse Per Second Signal

The GPS module outputs the Pulse Per Second signal at a precise time interval of one second. It is available as an RS-232 signal on the rear panel connector (P14) and the front panel connector (JP2). This signal has a pulse width of no more than 100 ms. Furthermore, the PCI based dual-channel UART bridge (used to implement the PCI interface) can be programmed to generate an interrupt on reception of the Pulse Per Second Signal.

6.8 Suported NMEA Sentences

The GPS receiver module supports the following NMEA sentences : GLL, GGA, RMC, VTG, GSV, GSA, ZDA. A brief overview of these sentences fol lows (consult the NMEA 0183 Interface Standard for further information on these sentences).

6.8.1 GGA : Global Positioning System Fix Data

6.8.1.1 Description :

Time, position and fix related data for a GPS receiver.

6.8.1.2 Sentence Structure :

$GPGGA,hhmmss.ss,llll.ll,a,yyyyy.yy,a,x,xx,x.x,x.x,M,x.x,M,x.x,xxxx*hh

6.8.1.3 Data Fields :

hhmmss.ss = UTC

llll.ll = latitude of position

a = N or S

yyyyy.yy = longitude of position

a = E or W

x = GPS quality indicator (0=no fix, 1=GPS fix, 2=Dif. GPS fix)

xx = number of satellites in use (0-12)

x.x = horizontal dilution of precision

x.x = antenna altitude above mean-sea-level, metres

M = units of antenna altitude, metres

x.x = geoidal separation, metres

M = units of geoidal separation, metres

x.x = age of Differential GPS data, seconds

xxxx = differential reference station ID (0000-1023)

hh = checksum : The absolute value calculated by exlusive OR-ing the 8 data bits (no start or stop bits) of each character in the NMEA sentence, between, but excluding '$' and '*'. The hexadecimal value of the most significant and least significant 4 bits of the result are converted to two ASCII characters (0-9, A-F (upper case)) for transmission. The most significant character is transmitted first.

6.8.2 GLL : Geographic Position - Latitude/Longitude

6.8.2.1 Description :

Latitude and longitude, time of position fix and status.

6.8.2.2 Sentence Structure :

$GPGLL,llll.ll,a,yyyyy.yy,a,hhmmss.ss,A*hh

6.8.2.3 Data Fields :

llll.ll = latitude of position

a = N or S

yyyyy.yy = longitude of position

a = E or W

hhmmss.ss = UTC

A = status, (A=valid, V=invalid)

hh = checksum (refer to 6.6.1)

6.8.3 GSV : GNSS Satellites in View

6.8.3.1 Description :

Number of satellites in view, satellite ID numbers, elevation, azimuth and SNR value.

6.8.3.2 Sentence Structure :

GPGSV,x,x,xx,xx,xx,xxx,xx.....,xx,xx,xxx,xx*hh

6.8.3.3 Data Fields :

x = total number of messages (1-9)

x = message number (1-9)

xx = total number of Satellites in View (SV)

xx = satellite ID number

xx = elevation, degrees

xxx = azimuth, degrees True (000-359)

xx = SNR (C/No) (00-99dB-Hz)

= 2nd-3rd SV

xx,xx,xxx,xx = 4th SV

hh = checksum (refer to 6.6.1)

6.8.4 RMC : Recommended Minimum Specific GNSS Data

6.8.4.1 Description :

Time, date, position, course and speed data provided by a GNSS navigator receiver.

6.8.4.2 Sentence Structure :

$GPRMC,hhmmss.ss,A,llll.ll,a,yyyyy.yy,a,x.x,x.x,ddmmyy,x.x,a*hh

6.8.4.3 Data Fields :

hhmmss.ss = UTC of position

A = status, (A=valid, V=invalid)

llll.ll = latitude of position

a = N or S

yyyyy.yy = longitude of position

a = E or W

x.x = speed over ground, knots

x.x = course over ground, degrees True

ddmmyy = date

x.x = magnetic variation

a = E or W

hh = checksum (refer to 6.6.1)

6.8.5 VTG : Course Over Ground and Ground Speed

6.8.5.1 Description :

The actual course and speed relative to the ground.

6.8.5.2 Sentence Structure :

$GPVTG,x.x,T,x.x,M,x.x,N,x.x,K*hh

6.8.5.3 Data Fields :

x.x = course over ground, degrees True

x.x = course over ground, degrees Magnetic

x.x = speed over ground, knots

x.x = speed over ground, km/hr

hh = checksum (refer to 6.6.1)